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(54) IMPROVEMENTS IN TAPE RECORD AND PLAYBACK SYSTEMS

(71) We, REDIFFUSION REDITRONICS LIMITED, a British Company of, La Pouquelaye, St. Helier, Jersey, Channel Islands, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to tape systems, and in particular to tape systems the operation of which can be automatically controlled.

In a known tape system an endless loop tape in cassette or any other endless loop format has an information signal recorded on one track and a control signal recorded on another track. The control signal track contains at predetermined intervals a tone burst of a duration which is determined at the time of recording. By controlling the length of this tone burst, two control functions are provided, one controlling tape drive so that the tape stops at the end of a particular section, the other controlling the record circuitry to inhibit recording of a subsequent section of the tape. The system is thus time conscious and responds accordingly.

The known system has been commercially applied but is essentially inflexible. For example, where the information signal comprises a series of individual pieces of music, it is not possible to make selections from the recorded pieces at random and therefore unwanted repetition cannot be avoided once a tape has been recorded. In particular, specific pieces of music cannot be located for playback.

It is an object of the present invention to provide a tape system which obviates or mitigates the above problems.

According to the present invention there is provided a tape recording and playback system comprising means for recording information signals on a tape, means for recording digital signals on the tape to identify selected tape segments and any information signals recorded thereon, means for playing back the recorded digital signals, and means for providing system-control-signals dependent upon the played back digital signals, wherein the digital signal recording means comprises an astable timing oscillator, a parallel to serial register receiving clock pulses from the timing oscillator, switches for supplying a binary digital code to the parallel inputs of the register, which digital code appears at the serial output of the register in response to received clock pulses, a data oscillator controlled by the serial output of the register to oscillate at a first or a second frequency in dependence upon the state of the serial output of the register, and a clock oscillator arranged to oscillate at a third frequency, the outputs of the data and clock oscillators being combined to provide a common output comprising a series of pulses at the first or second frequency separated by pulses at the third frequency.

In one embodiment, the second frequency is zero.

The information signals and digital signals may be recorded on separate tracks, or alternately on a single track in different frequency bands.

The control signals essentially identify predetermined segments of the tape and may be used for a wide variety of control purposes, for example to start/stop tape playback, to control tape playback so that selected tape segments are played in any desired sequence whereas other tape segments are ignored, to control tape transport speed, or to control auxiliary equipment such as auxiliary tape machines.

The present invention also provides a method of controlling a tape recording and playback system in dependence upon a tape which is being played back by a tape recording and playback machine which is a component of the system, wherein digital signals are recorded on the tape to identify selected tape segments and any information signals recorded thereon, the recorded digital signals are played back, and system-control-signals are provided in dependence upon the played back digital signals, wherein in order to generate said digital signals an astable timing oscillator

provides clock pulses to a parallel to serial register, the parallel inputs of which are supplied with a binary digital code by switches, which digital code appears at the serial output of the register in response to the clock pulses, a data oscillator is controlled by the serial output of the register to oscillate at a first or a second frequency in dependence upon the state of the serial output of the register, a clock oscillator is arranged to oscillate at a third frequency and the outputs of the data and clock oscillators are combined to provide a common output comprising a series of pulses at the first or second frequency separated by pulses at the third frequency.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figures 1 to 3 illustrate tape encoding circuitry;

Figure 4 illustrates waveforms appearing in the circuitry of Figures 1 to 3;

Figures 5, 6 and 7 illustrate decoder circuitry;

Figures 8 to 12 illustrate auxiliary circuitry controlled or operating in conjunction with the circuitry of Figures 5, 6 and 7;

Figures 13 and 14 schematically illustrate alternative circuits to those shown in Figures 5 to 12; and

Figures 15 and 16 show additional circuitry for connection to the circuitry of Figures 8 to 12.

The control circuits of the unit described below with reference to the drawings provide the following functions:

(i) To control the motion of the magnetic tape across the recording/reproducing and erase heads of the machine.

(ii) When the unit is in the monitor or playback modes, to display the identification code of the information which is to be played back next (tape stationary) or is being played back (tape in motion).

(iii) When the unit is in the record mode, to display the identification code which is allocated to the information about to be recorded (tape stationary) or is being recorded (tape in motion).

(iv) Additionally in the record and monitor modes, to provide an indication as to whether a recording can be made or whether the location chosen is reserved for a prerecorded recording which cannot be over-recorded. In the latter case a bias and erase oscillator is disabled and the recording amplifier is disconnected from the recording head.

The control functions are set up by the circuits in response to pre-recorded coded information recorded on a separate control track of the tape which is monitored, in the playback mode, irrespective of the mode of operation of the main amplifier of the unit.

The coded information takes the form of seven short periods of signal at a frequency f1. corresponding to a logic level '1', or of no signal, corresponding to a logic '0', each period being followed by an equal period of signal at a second frequency f2. Whether the signal f1 is present or not during each of the seven period is determined by the logic level of the relevant bit of the BCD (Binary Coded Decimal) code of the identification code. (As an example, if the identification code is 39, the BCD code for this is 0111001, and the signal on the tape would be f1, f2, –, f2, –, f2, f1, f2, f1, f2, f1, –, f2. Note. The least significant bit (LSB) is transmitted first).

An eighth period of signal frequency f1, if the location corresponding to the identification code may be recorded on the unit, or of no signal, if local recording is inhibited, is followed by a long period of signal frequency f2. Although the length of this last period need only be in the order of twice the short period, the period is chosen to be approximately one hundred times the short period if local recording is inhibited and approximately five hundred times the short period if local recording is allowed, in order that tapes recorded for use on the described unit may be compatible with existing playback machines.

The response of the audio amplifier and the routing of the signal within the playback unit vary depending upon the mode of operation of the unit. Except where the signal amplitude is too great, this change of response and signal routing is achieved by means of solid state analogue switches.

These switches are controlled by d.c. voltages derived from the mode selection logic. The particular voltages present at any time will depend upon the mode selected, a press-to-talk switch and control signals read from the tape.

In the following circuit descriptions a positive logic nomenclature is used where logic level '1' is equivalent to the positive supply rail of the logic circuits and logic level '0' is equivalent to the negative rail.

Referring to Figure 1 the timing of the duration of the frequency bursts representing the coding pulses is determined by a gated astable oscillator formed by components 1 and 2. When an initiate switch 3 is closed by the unit operator a pulse is generated by a monostable oscillator formed by components 4, 5 which changes the state of an oscillator gating bistable 6 allowing the timing oscillator 1, 2 to operate.

The initial state of the oscillator output appearing at terminal 7 is logic level '1', and therefore the state of the output of an inverter 8 appearing at terminal 9 is logic '0'. When the oscillator starts the inverter output changes the level '1', and this transition causes a divider 10 (Figure 2) to change from its initial state in which it provides a logic '0' output to a state in which it provides a logic '1' output. This change of level is applied to the clock input of a parallel to serial buffer register 11. Upon

receipt of the clock pulse from the divider 10 the data states applied to the parallel inputs of the register 11 by means of set spot number switches 12, 13 and record inhibit/enable switches 14, are fed into the buffer. This occurs since the circuit is held in the parallel mode by the initial state of a parallel/serial bistable 15.

A half cycle later the output 16 of a divider 17 changes state, the output rising from level '0' to level '1' and thus changing the state of the parallel/serial bistable 15 to switch the buffer register 11 to the serial mode of operation.

At the same time the output 18 of the divider 17 goes to logic level '0' enabling a data gate 19, thus allowing the logic level at the output of the buffer register 11 to be transferred via inverter 20 and data gate 19 to terminal 21. The terminal 21 is connected to the control input of a gated data oscillator 22 (Figure 3). If a logic '1' is present at the output of buffer 11 (Figure 2), this will cause the data oscillator 22 to oscillate at a frequency f1. If the buffer output is at level '0' then the data oscillator is inhibited from oscillating.

One complete cycle of the gated oscillator 22 later, the outputs of the divider 17 (Figure 2) change state again. The output 18 rises to logic '1' closing the data gate thereby inhibiting the data oscillator 22 (Figure 3). The output 16 which is at logic level '0' is applied to a clock gate 23 whose other input is derived from the output of the parallel/serial bistable 15. As this output is at level '0' both inputs to the clock gate are at level '0' and the output applied to terminal 24 will be logic '1'. This output gates the gated clock oscillator 25 (Figure 3) which oscillates at a frequency f2. The logic '1' from the clock gate 23 is applied also to the input of a counter 26 (Figure 2) which advances one count.

A half cycle later the output 16 of the divider 17 again rises from logic '0' to logic '1'. This transition, applied to the clock input of the buffer register 11 causes the information held in the buffers to advance one position transferring the data state of the penultimate buffer to the inverter 10.

The above sequence, except for the change from parallel to serial operation of the buffer 11 is repeated for every two cycles of the gated oscillator 1, 2 (Figure 1) until the counter reaches a predetermined count, in this case eight.

When the eighth clock pulse is gated the counter reaches the count 'eight' and the corresponding output 27 rises to level '1' triggering, via inverter 28, a long tone timer 29. When triggered the output 30 of the timer 29 rises to level '1', maintaining the gated clock oscillator 25 (Figure 3) via terminal 24 and resetting the oscillator gating bistable 6 (Figure 1) via terminal 31. The signal applied by the bistable 6 to the oscillator component 1 rises to logic '1', stops the gated oscillator 1, 2 and resets the dividers 10 and 17 (Figure 2). Divider 17 in turn sets the parallel/serial bistable 15 to the state corresponding to parallel operation of the buffer 11 and sets the counter 26 to the zero count state.

The time for which the output of the timer 29 stays at level '1' depends upon the state of the record inhibit/enable switch 14. If recording is to be allowed the timer 29 stays on for approximately five times the duration of the output provided if recording is to be inhibited. This feature is to enable tapes encoded for use with this equipment to be played on prior art equipment.

If required the function of the record inhibit/enable switch 14 may be carried out by a biased push button 32 and memory bistable 33 (Figure 2) which is automatically reset after each encoding operation. This feature prevents the record enable code being recorded accidentally if the operator fails to reset the record enable switch.

The voltage appearing at terminal 34 (Figure 2) which is connected to bistable 6 (Figure 1) via terminal 35, the voltage appearing at terminal 36 (Figure 3) and the voltage appearing at terminal 37 (Figure 2) are applied to indicating devices to enable an operator to monitor the encoding process.

Figure 4 illustrates waveforms appearing in the circuitry of Figures 1 to 3, the waveforms being identified by reference numerals corresponding to the reference numerals of components at the outputs of which the respective waveforms appear. The illustrated waveforms correspond to the identification code selected by switches 12, 13 being 99 so that the signal appearing at output 38 comprises alternate bursts at frequencies f1 and f2 with no gaps, i.e. f1,f2, f1,f2, f1,f2, f1,f2, f1,f2, f1,f2, f1,f2.

A particular "spot" on a tape may be identified with a selected code by manipulating switches 12, 13 and actuating switch 14 (or 32). The output at terminal 38 is applied to recording heads (not shown) which cause the code signal to be recorded on a separate track of the tape from that carrying information signals such as music. When the tape is played back the recorded coded signals are also played back and applied to control circuitry as described below.

Figures 5, 6 and 7 illustrate elements of a decoder circuit for processing played back identification codes.

Referring firstly to Figure 6, when the decoder circuit is first switched on, an initial set up network formed by capacitor 39 and resistor 40 provides a positive pulse to a data pulse delay bistable 41 the output 42 of which is thus set to logic '0'. In addition, the outputs of a data memory shift register 43 are set to logic '0', thereby causing conventional displays 44 fed via decoders 45 to show 00, output 46 of a record enable latch bistable 47 is set to logic '0', thereby inhibiting local recording by causing 48 to remove a "record enable" signal

from terminal 49, and output 50 of a drive control latch bistable 51 is set to logic '0', thereby applying a signal to terminal 52 to switch off a drive motor 53 and drive solenoid 54 (Figure 7).

When a start pulse, is applied to terminal 55 (Figure 6), which start pulse may be initiated by either a microphone switch or a timer, it appears at the reset output 56 of the drive control latch 51 which as a result changes state. The logic '1' appearing at output 50 is applied via terminal 52 and current amplifier transistor 57 (Figure 7) to the gate of a triac 58 which switches on. This applies a.c. power to the synchronous drive motor 53. Simultaneously the output 50 is applied via terminal 52 to a solenoid delay circuit 59, 60 and 61 which, after a delay determined by resistors 62, 63 and capacitor 64 to allow the drive motor 53 to attain its terminal speed, switches on transistors 65 and 66 pulling in the solenoid 54 and thus starting the tape. The solenoid 54 is driven from a power supply having poor regulation, but the charge stored in capacitor 67 is sufficient to cause the solenoid to pull in while the current available from the power supply is sufficient to retain the solenoid in the operated position.

The negative transition of the output 68 of the drive control latch bistable 51 (Figure 6) triggers a start pulse inhibit timer 69, the output 70 of which is applied to one input of a drive control gate 71, preventing the output of a long pulse detector formed by component 72 and transistor 73 from changing the state of the drive control latch bistable 51 during the time the 'compatible' tone is present. The timer output 70 is applied also to the reset terminals of the data pulse delay bistable 41 and date memory 43 to cancel any information held in these registers. This latter function is redundant for the first operation after the unit has been switched on since the initial set-up network will have zeroed both registers but is required for subsequent operations.

The tape will continue to run allowing the tape to be played back but for the first operation it is not possible to record as the record enable latch 47 is set to record inhibit.

The pre-recorded control signals on the tape induce a voltage in a replay head connected to terminals 74 (Figure 5) which is amplified by amplifiers 75 and 76. The gains of the amplifiers are determined by resistors 77 and 78 for amplifier 75 and by resistors 79 and 80 for amplifier 76. Capacitors 81, 82 and 83 are included to reduce the amount of stray bias signal applied to subsequent stages when the unit is in the record mode. The output of the amplifiers is fed, via a low pass filter formed by resistor 84 and capacitor 85 and d.c. blocking capacitors 86 and 87 to two frequency selective switches 88 and 89 which are effective as pulse detectors.

The frequency selective switches 88 and 89 provide a logic '1' output whenever the frequency of the input signal is within preset limits. The upper frequency limit of the data pulse detector 88 is determined by the network formed by resistors 90, 91 and capacitor 92 and preset to f1 plus 10% while the lower limit is determined by resistors 93, 94 and capacitor 95 and set to f1 minus 10%. Similarly the upper frequency limit of the clock pulse detector 89 is determined by resistors 96, 97 and capacitor 98 and chosen as f2 plus 10% and the lower limit is determined by resistors 99, 100 and capacitor 101 and chosen as f2 minus 10%. In order that drop-outs of the signal on the tape do not cause the switches to detect false pulses, the outputs of the switches are prevented from reverting to logic '0' during signal absences shorter than a preset period determined by the networks formed by components 102, 103 and 104, 105. Diodes 106, 107, 108 and 109 prevent excessive inputs damaging the frequency switches 88, 89.

If a data pulse of frequency f1 is present on the tape, this will cause the output of the data pulse detector 88 to go to logic '1' which in turn will cause, via terminal 110, the data pulse delay bistable 41 to switch such that output 42 goes to logic level '1' (see Figure 6). The following clock frequency f2 on the tape will cause the output of the clock pulse detector 89 to go to logic '1'. This output is applied to the clock terminal of the data memory 43 and causes the logic '1' on the output 42 of the data pulse delay bistable 41 to be transferred to the first register of the data memory 43.

If the clock frequency f2 is preceded by no signal, the data pulse detector 89 and the output 42 of the data pulse delay 41 remain at logic level '0'. Therefore, a logic '0' is transferred to the first register of the data memory 43.

The logic '1' at the output of the clock pulse detector 89 is applied to a clock pulse delay circuit formed by components 111, 112 and 113. The clock pulse delay input is fed via buffer transistor 114 which prevents the clock pulse delay circuit slowing the rise time of the output of the clock pulse detector 89. The inputs of components 111 and 112 are held at logic '0' by resistors 115 and 116, and therefore their outputs are at logic '1'. When the output of the clock pulse detector 89 rises to logic '1' the input of component 111 rises for a period determined by resistor 115 and capacitor 117. Thus the output of component 111 is a negative pulse. As the output of component 111 rises to logic '1' at the end of the pulse the input of component 112 is forced to logic '1' for a period determined by resistor 116, and capacitor 118. The negative output pulse is applied to the inverter 113 whose output is a positive pulse whose width is governed by resistor 116 and capacitor 118, delayed by a time determined by resistor 115 and capacitor 117.

This pulse resets the output 42 of the data pulse delay bistable 41 via terminal 119 after the data has been transferred to the data memory 43 and prior to the receipt of the next data period.

The preceding sequence is repeated for all eight data and clock periods. On receipt of each clock pulse the information stored in each register of the data memory is transferred to the next register in the store 43. Thus for example after eight clock pulse the logic level of the first data period will be stored in the eighth register and the logic level of the last data period will be stored in the first register.

The output of the clock pulse detector 89 is applied also to the long pulse detector formed by components 72, 73 the output of which goes negative whenever a clock pulse occurs which is longer than a preset period, determined by resistor 120 and capacitor 121. When the long eighth pulse is detected the output of the long pulse detector, which is logic '0', causes the output of the drive control gate 71 to go to logic '1', provided the period set by start tone inhibit timer 69 has elapsed.

The logic '1' at the set input of the drive control latch 51 causes it to change state, switching off the drive motor 52 (Figure 7) and releasing the drive solenoid 53 instantaneously. The drive control gate output is applied, via inverter 122, to the latch enable inputs of latches of the display decoders 45, transferring the data in registers two to eight of the data memory 43 into the decoders 45 which convert the BCD code to a form suitable for driving the seven segment displays 44, thus updating the spot number display. Once the tape stops the output of the drive control gate 71 goes to logic '0' enabling the data in the data memory 43 to be altered without altering the display.

The positive transition of the output of the drive control latch 51, as the bistable changes state, is applied to the clock input of the record enable latch 47, causing the data on the first register of the data memory 43 to be transferred to the output 46 of the record enable latch 47. If this is a logic '0', this signal is taken via terminal 123 (Figure 6) to a record bias and erase oscillator power supply (Figure 8) and prevents the power supply from being switched on in the record mode. This happens because the bias current of a supply switching transistor 124 is not supplied by components 125, 126. If logic '1' is present at terminal 123, base current is available and it is possible to obtain bias and erase current in the record mode. The logic '0' signal at the output terminal 127 of the record enable bistable 47 (Figure 6) is fed to the switch logic (Figure 9) allowing a recording amplifier (Figure 10) to be connected to the recording head.

The logic '0' signal at the output 56 of the drive control latch 51 is fed to the trigger input of a timer 128 (Figure 11) to initiate the timer in the auto mode.

Diodes 129, 130, 131, 132 and 133 (Figure 6) buffer the outputs of the gates and other components during set-up and reset operations. Diodes 134, 135 (Figure 6) and 136 (Figure 7) prevent the logic '0' exceeding the reverse base-emitter voltage of the relevant transistors if split supplies are used.

A microswitch 137 (Figure 6) presets the control circuit to the initial set-up state whenever a tape cassette is ejected from the tape mechanism.

The operational modes of the tape recorder unit are selected by operation of interconnected push button switches shown in Figure 9. In normal operation when a button is depressed that particular switch latches into position and any other switch which was engaged releases. It is possible to partially depress a button, causing the other switches to release, so that it falls to latch and upon release of this button a situation arises where no switch is selected. Conversely it is possible to depress two buttons together when both switches will latch. It is the purpose of this circuit to prevent operation of the unit when either of these false conditions exist.

Each of selector 138, 'RECORD', 139 'MONITOR' and 140 'AUTO' has one terminal taken to logic level '0' and the other taken to the input of respective inverter 141, 142 and 143. These inputs are normally held at logic '1' by resistors 144, 145 and 146 respectively. Therefore the outputs of the inverters will be at logic '0' until a selector switch is engaged when the output will change to logic '1'.

Associated with each selector switch is a three input NOR gate 147, 148 and 149 respectively, one input of which is from the associates switch, the other inputs being from the outputs of the inverters associates with the other two switches.

If only one switch is pressed the gate connected to the switch will go to logic '0' and the output of the inverters connected to the other two switches will be at logic '0' also. Hence all three inputs to the gate will be at logic '0' and the output will be logic '1'. The output of the inverter connected to the actuated switch will be logic '1' and this will prevent the outputs of the other two gates going to logic '1'.

When more than one button is depressed or when no button is depressed, all three gates will have at least one input at logic '1' preventing any output rising to logic '1'. Thus when one, and only one, button is engaged, there will be a logic '1' output at the associated gate.

For convenience these logic '1' outputs when the record, monitor and auto switches are operated will be referred to as outputs 150, 151 and 152 respectively.

As the current drawn from the output 152 is greater than can be supplied by the logic gate this supply line is fed from a current amplifier transistor 153.

Whenever a logic '1' is present at the output of a gate, a logic '1' will be present also at the

junction of diodes 154, 155 and 156. This voltage, referred to as output 157, is fed to an external microphone switch (not shown) via terminal 158 under the control of the equipment user.

When the record switch 138 is selected, output 150 is applied to the input of an inverter 159 the output of which is fed to one input of a three input NOR gate, 160. Another input to this gate if fed via terminal 161 from the record enable latch 47 (Figure 6) which is at logic '0' whenever the code recorded on the tape allows for a recording to be made. The third input is taken, via terminal 162 and inverter transistor 163, from a press-on-talk switch on the microphone (not shown). Normally the input to the inverter 163 is held at logic '0' by resistor 164, but whenever the press-to-talk button is pressed a logic '0' appear on the third input of the gate.

Thus whenever the unit is in the record mode, the coding allows for a recording, and when the press-to-talk button is pressed, a logic '1' is present at the output of component 160.

When the press-to-talk switch is operated in either the record and monitor modes, a signal is applied via either the record switch 138 or monitor switch 139 to a pulse generator formed by components 165, 166. The positive pulse generated by this circuit is applied via terminal 55 to the reset terminal of the drive control latch 51 (Figure 6), starting the tape drive.

When the press-to-talk switch is operated in the Auto mode output 157 is applied via the auto switch 140 and inverter 167, to one input of a three input NOR gate 168. A further input receives output 151, which is logic '0'. The third input is connected to logic '0' by resistor 169, thus all inputs are at logic '0' and therefore the output of the gate is logic '1' (referred to as output 170).

If a link 171 is connected via terminal 172 to the output 50 of the drive control latch 51 (Figure 6) and to the input of the gate 168, the logic '1' present whenever the tape drive is engaged prevents output 170 from being generated. The link 171 thus controls the priority of the paging system, the priority being "microphone over spot" when the link is not present, and "spot over microphone" when the link is present.

The outputs 150 and 170 are combined in an AND gate formed by diodes 173 and 174 to provide a control voltage referred to as output 175.

The drive control latch 51 (Figure 6) is switched, in the auto mode, to the on state by the timer 128 (Figure 11) which is initiated by the negative transition of the output 50 of the drive control latch 51 via terminal 172.

Control voltages appearing at the output of component 160, outputs 175 and 151, and the output of the timer 128 combined with output 170 are used to control the signal routing switches of the main audio amplifier.

Both the control voltage 170 and the output of the timer 128 will switch a interface relay 176 (Figure 11) which is used to control external amplifiers whenever paging or spot announcements are being made.

Indicator diodes 177, 178 and 179 are controlled by transistors 180, 153 and 181 to indicate which mode of operation has been selected.

Amplication of the signals from the microphone (not shown) or the head section 182 (Figure 10) is carried out by components 183, 184, 185 and 186. These signals are routed by the quad analogue switches 187, 188, 189, 190 and 191, 192, 193, 194 as directed by the mode selection logic. Switch 187 is connected via terminal 195 to the output of gate 160 (Figure 9), switch 191 is connected via terminal 196 to output 175 (Figure 9), and switch 192 is connected via terminal 197 to the circuit of relay 176 (Figure 11). Switches 193 and 194 are connected via terminal 198 to output 151 (Figure 9).

In the replay mode the signal from head 182 is coupled through capacitors 199 and 200 to the input of the first amplifier section 183 when the relay contacts 201 are closed. The control voltage 175 (Figure 9) is at logic '0' which causes transistor 202 to activate relay 203 and also opens the analogue switches 189 and 190. Capacitor 204 resonates with the playback head at a high audio frequency to provide some high frequency lift and a more rapid roll-off above this frequency to reduce noise.

The gain of amplifier 183 is set by resistors 205, 206 with capacitor 207 reducing the gain above the audio range to ensure stability. The bias at the input of amplifier 183 is provided by resistors 208, 209 with capacitor 210 decoupling resistor 209 to maintain a high input impedance. Positive supply is via resistors 211 and 212.

The second stage providing gain is 186. The gain and frequency response for equalisation are controlled by resistors 213, 214, 215 and capacitor 216. In the replay mode output 175 (Figure 9) is at logic '0' so that switch 191 is open and resistor 217 has no effect on the circuit. Capacitor 218 de-couples the earthy end of resistor 215. Resistor 219 allows capacitor 218 to be charged quickly to its final operating voltage when the unit is switched on and also provide additional low frequency roll-off. The input bias for switch 186 is derived from the potential divider 220, 221. Capacitor 222 ensures high frequency stability.

The supply to amplifier 183 and for the input bias to amplifier 186 is given additional filtering by amplifier 184, resistor 223 and capacitor 224.

When the signal at the output of amplifier 186 exceeds about 900mV, amplifier 185 forms a potential divider with resistor 225 to

reduce the signal reaching the input of amplifier 186 through the coupling capacitors 226 and 227 from amplifier 183. This forms an automatic level control circuit with the attack time depending on resistor 228 and capacitor 229 and the decay time depending on resistor 230 and capacitor 231.

An amplifier 232 provides further gain to the signal path according to the ratio of resistors 233 and 234. Capacitors 235 and 236 are the input and output coupling capacitors. Amplifier 232 is also a mixing stage to mix a signal appearing at terminal 237 from a chime generator (Figure 12) into the signal path via capacitor 238 and resistor 239. In this case the gain for the chime signal is the ratio of resistor 239 to resistor 234. In both cases capacitor 240 provides additional high frequency roll-off. The output signal from capacitor 235 is connected to an output level control 241 which is adjustable from the front panel.

If the unit is in the auto mode switch 192 will be switched on by the timer 128 (Figure 11) or during paging to allow the signal from the slider of the output level control 241 via capacitor 242 to reach amplifier 243 which is a current amplifying output driver, coupled by capacitor 244 to the output terminal 245. The output terminal 245 and terminals 246 (Figure 11) are connected to an output socket (not shown).

In other modes the signal paths are modified by the states of the mode selection logic controlling the quad analogue switches 187 to 194.

In the record or paging modes the playback head 182 (Figure 10) is isolated from the input of the amplifier 183 by opening the contacts 201. In this case the control for switches 189, 190 and 191 is at logic '1' so that input to amplifier 183 is derived from the microphone socket (not shown) via terminal 247. The signal is coupled via capacitors 248 and 200. Capacitor 248 and resistor 249 form a low pass filter to improve speech intelligibility. Switch 191 connects resistor 217 in parallel with resistor 214 and capacitor 216 to provide the required record characteristic.

Switches 187 and 188 can with inverter transistor 250 form a single pole double throw switch so that when recording, with the output of gate 160 (Figure 9) at logic '1', the signal at the output of amplifier 232 is connected via 251 and capacitor 199 to the head 182.

In the monitor mode the output from amplifier 232 is switched through 193 and 194, in parallel, to the microphone socket via terminal 247 and capacitor 252 so that it is possible to monitor the recorded signal using the microphone as an earphone.

The timer circuit (Figure 11) provides, in the 'AUTO' mode, automatic repetitive initiation of the drive control pulse circuit at preselected timed intervals of between two and twenty minutes between spots. Intervals are selected using switch 253.

In order to maintain stable and accurate timing timer 128 contains an oscillator and a twelve stage binary divider which times out after 4095 counts, eliminating the need for large time constants.

The supply for the timer is taken from the emitter of transistor 153 (Figure 9) via terminal 254, and therefore only operates in the Auto mode. The timer has an internal zener diode, supplied by resistor 255 and de-coupled by capacitor 256.

The time period is set by switch 253 which selects an appropriate combination of resistors to form the time constant with a capacitor 257. Resistor 258 trims the frequency for calibration. Capacitor 259 suppresses external noise which might cause false triggering of the oscillator.

The timer 128 is started by a negative going pulse from the drive control latch 51 (Figure 6) via terminal 172 which is the transition from logic '1' to logic '0'. Diode 260 prevents the trigger point of the timer from loading latch 51 when at logic '1'.

Transistor 261 acts as a level shifter as well as an inverter and provides a signal fed to transistor 262 of an interface relay driver and via terminal 263 and the mode selection switch 138 (Figure 9) to the drive control pulse gate 165.

The bias and erase oscillator (Figure 8) consists of transistors 264 and 265. Resistors 266, 267, 268 and 269 provide the d.c. bias. The emitter resistors 270 and 271 limit the current in this stage. The frequency of oscillation is determined by the inductance of the erase head 272 and by capacitor 273. The feed back path to maintain oscillation is via capacitor 274 and diodes 275, 276.

For recording, bias is applied to the head 182 (Figure 10) via terminal 277 and capacitors 278,

The d.c. supply is switched to the oscillator via transistor 124 which is itself controlled by components 125, 126 and 279 connected to form an AND gate so that the oscillator can only oscillate when the record mode is selected, (output 150 (Figure 9) at logic '1') and also when the control output terminal 280 of the record enable latch 47 (Figure 6) is at logic '1'.

The interface relay is 281 (Figure 11) is provided to cue associated equipment. It is activated by a logic '1' from the timer 128, or in 'paging' mode, via diodes 282 with the emitter follower 262. The contacts 176 provide a short circuit between terminals 246 which are connected to the output socket (not shown).

The chime generator (Figure 12) provides a sequence of two bell-like notes preceding a spot or a paging announcement to attract attention.

A logic '1' at terminal 263 or 283 (Figures 9 and 11) will switch transistor 284 via terminal 285 (Figures 11 and 12), diode 286 or 287 to give a logic '0' at the input of inverter 288. The

resultant logic '1' at the output of inverter 288 is transferred to the input of component 289 for a period depending on the time constant of capacitor 290 and resistors 291, 292. A negative pulse is generated at the output of component 289, (logic '0'). When this returns to logic '1', a second negative pulse is generated at the output of component 293 the duration of which is dependent on the time constant of capacitor 294 and resistors 295, 296. These two pulses form the controls for the chimes.

During the first pulse the circuit formed by components 297, 298 will oscillate at a first frequency. During the second pulse the circuit formed by components 299 and 298 will oscillate at a second frequency. Oscillations cease at the end of the second control pulse or if the collector of transistor 284 returns to logic '1'.

The leading edge of each control pulse also momentarily switches on transistors 300 and 301 sequentially allowing capacitor 302 to charge via resistor 303 to the supply voltage followed by a slow discharge through resistor 304.

The voltage across capacitor 302 causes the oscillations from component 298 to be transferred through the diode gate 305, 306 to resistor 307 with a decaying amplitude dependent on this voltage and the ratio of resistors 308, 307. The oscillation is still a square wave and is filtered by transistor 309 with its associated components to produce a sinusoidal waveform with a pleasing tone.

Resistor 310 is adjustable from the front panel to set the level of the chimes via terminal 237 (Figure 10).

The chimes are normally initiated at the start of a spot or paging announcement. If the chimes are required for one state only, removal of diode 286 (Figure 11) will inhibit the paging chimes or removal of diode 287 will inhibit the spot chimes.

Figure 13 illustrates an alternative arrangement to that shown in Figure 6. This alternative circuit gives the user the option of displaying an elapsed time, in seconds, during recording.

The outputs of the data memory 43 (Figure 6) instead of being taken to the display decoders 45 directly, are fed to the inputs of data stores 311, 312, 313, 314, 315, 316 and 317. These circuits store, and present at their outputs, the information present at the inputs during the positive transition of the clock input voltage. Whenever the output of the drive control gate 71 (Figure 6), goes to logic '1', i.e. on receipt of a stop signal, the data in the data memory is transferred to the data stores where it is retained until the receipt of the next stop pulse. The data store outputs are fed to one set of inputs of display select gates 318 and 319.

A main frequency signal, derived from the mains supply, is fed to the input of a divider counter 320 which provides an output once per second. This is fed to a seconds display counter, 321, which provides a BCD coded output representing the elapsed count. The outputs from this counter are fed to the second set of inputs of the display select gates 318, 319.

When the unit is first switched on a spot/time select bistable, 322 is set so that the Q and $\bar{Q}$ outputs set the display select gates outputs to correspond to the first set of inputs, indicating the code held in the data stores 311 – 317. At the same time a blanking bistable, 323, is set so that its output enables the display input of display decoders 324 and 325. Thus the display will display the tape location code.

When the unit is in the record mode, a recording is allowable if a 'time' switch 326 is pressed. The spot/time and blanking bistables 322, 323 change state. This causes the seconds counter 321 output to be selected by the display select gates 318, 319 and fed to the display decoders 324, 325. However this is set to the blanked mode therefore no display is presented by the display devices.

Once the tape drive engages, a reset potential is applied to the divider 320 and the counters start. After a time, determined by a time delay counter 326, a signal is applied to the blanking bistable 323 enabling the display to light up. The lighting up of the display may be used as an indication that recording may commence and the elapsed time of the recording is displayed.

At the end of the recording, either because a stop pulse is generated by the drive control gate 71 (Figure 6) connected to terminal 327 or upon release of the 'press to record' button by the user, when an end of recording detector 328 generates an output pulse, the spot/time select bistable 322 will change state causing the display to show the last identification code generated from the tape. Terminals 329, 330 and 331 receive the outputs of gate 160 (Figure 9), 149 and 148 respectively. Terminals 332, 333 and 334 receive an initiating signal, a solenoid delay signal from the delay circuit of Figure 7 and mains voltage respectively. When this circuit is included the latching function of the display decoder latches is not used.

Figure 14 shows an incomplete tape reset circuit. This circuit allows the user to record part of a tape and, upon playback, cause the unit to run on after playing the last recorded message (spot) until the first message is available for replay.

The output from the data memory 43 (Figure 6) is fed to the data stores 311 – 317 in the same manner as for the circuit of Figure 13. The outputs from the data stores are fed to terminals 335 of a last spot detector circuit 336 where it is compared with the code for the 'last recorded message' applied to terminals 337 which the user sets by means of last spot switches (not shown).

If the code read from the tape is less than or

equal to the code set on the last spot switches, the output from the last spot detector 336 is logic '0', and this is applied to inverter 338. The logic '1' from the inverter 338 is applied to stop pulse inhibit gate 339. The logic '1' on the input of 339 causes its output, which is applied to gate 340, to be logic '0'.

A positive stop pulse from the drive control gate 71 (Figure 6) is inverted and delayed, by stop pulse delay, circuits 341 and 342. The delay is of sufficient length to allow the output of the last spot detector 336 to settle. On receipt of the negative delayed stop pulse, both inputs of gate 340 are at logic '0' and therefore the output will rise to logic '1', changing the state of the drive control latch 51 (Figure 6) and switching off the drive.

After the last selected spot the code for each subsequent indentification will exceed the code set by the last spot switch and the output of the last spot detector 336 will rise to logic '1'. This will result in the input to gate 339 from the inverter 338 being logic '0' and, if the other inputs are at logic '0' also, the output will be logic '1'. This will force the output of gate 340 to logic '0', preventing stop pulses reaching the drive control. The tape will continue to run until the first spot is reached when the code from the tape will be less than that set on the last spot switches and stop pulses will again stop the tape.

So that centrally prerecorded messages cannot be missed by setting the last spot switches to a code less than that of these messages, a logic '1' is fed from the record enable latch 47 (Figure 6) whenever a centrally recorded message code is detected to gate 339 preventing the stop pulse inhibit gates 339, 340 from inhibiting the stop pulse.

Similarly logic '1' is applied to gate 339 whenever the unit is in the recording and monitor modes. Thus the tape may only run-on in the playback mode.

Whenever the tape is running-on, a logic '1' is fed from the output of gate 339 to the switching logic in order to prevent any audio output and preventing the interface relay operating.

A further addition, not shown, may be incorporated whereby the logic '1' output of the last spot detector 336 initiates a fast forward wind. In this case an additional signal will be necessary on the tape prior to the coded information for the first spot which will cause the unit to revert to normal speed.

The described circuitry may be adapted to provide further facilities. For example, by adding a switch facility a particular segment of a recording may be selected. Thus by comparison of the coded output from the tape with preset information, stored for example in a digital store, the mechanism can be instructed to automatically search for a particular segment of the tape identified by the preset information and subsequently to set iself for playback. The mechanism can of course automatically replay the selected segment rather await further instructions. If several such selection facilities are provided, a sequence of predetermined segments may then be automatically played back either with minimum delay or by utilisation of the internal timing facilities at preset intervals.

Conversely the omission of certain segments may be more appropriate to a particular requirement.

A particular application of this system couples the coding at the time of origination of a programme signal with a random number generator so that replay of the selected segments may be in a random order. This can be utilised to give a very large number of programme combinations from a relatively limited number of segments.

Although the above described systems generally suggest the use of numeric display, extension of the system to alpha display may be readily achieved and this may be of application in music systems for example. Further applications for the system include audio/visual equipment where the control or coded information derived from a tape may be utilised to control a number of projectors, possibly with cross-fade facilities.

Referring to Figure 15, a circuit for omitting spots on playback will be described.

It is possible for a user of the equipment, who has recorded a sequence of spots on a tape, to wish to miss out one of the announcements, for instance if the announcement relates to a product advertisment and the product is no longer available.

With the basic equipment it would be necessary to re-record the tape substituting a new spot in place of the unwanted one. It is the purpose of the circuit of Figure 15 to allow the user to omit selected spots provided these spots have been recorded locally. This proviso has been added since spots provided by the originator of the tape programme, and which cannot be erased by the user, may have been paid for and thus should not be omitted.

Although the circuit could be built to allow any number of spots to be omitted, due to the limitations of space for selector switches the practical application of the circuit is for a unit on which any iof spots 00 to 09 may be omitted.

Each time the equipment control circuitry detects a stop (clock frequency) pulse, the Q output of the drive control latch changes from logic '1' to logic '0'. This negative transition is transferred via terminal 343 and capacitor 344 to the clock inputs of data stores 345 and 346 and, upon receipt of this pulse, the data held in data memory 347 is copied into the data stores. Inputs indicated by numeral 348 are taken from the data memory 43 (Figure 6).

The outputs from the stores 345, 346 in the case of stores 345 and of the three date lines stores 346 corresponding to the tens digit of

the spot code, is the data copies into the store as the tape drive ceased. In the case of the line corresponding to the 'record enable' data bit the output is the complement of the data copied into the store.

The output of store 345 is fed to a BCD – to – decimal decoder 349. For each spot one of the '0' to '9' outputs of decoder 349 will be at logic level '1' depending upon the unit digit of the spot code. These output lines are fed via isolator diodes 350 to the user selectable spot omission switches. Any switch, which the user has operated in order to omit the spot corresponding to that switch, connects the corresponding output line to the input of a inverter 351 which in turn is fed to one input of a three input NOR gate 352.

Thus, if the unit digit of the spot code held in the data store corresponds with a switch that has been operated by the user, the input to gate 352 will be a logic '0', and in all other cases a logic '1'. A second input of the three input NOR gate 352 is taken from the date lines of store 346 corresponding to the 'tens' digit of the spot code via the NOR gate formed by diodes 353. This input will be at logic '0' if the spot number is 09 or less, and logic '1' if the spot number is 10 or greater.

The third input to gate 352 will be at logic '0' if local recording is allowable, and at logic '1' if local recording is inhibited.

The output of gate 352 will be logic '1' if the spot number is between 00 and 09, local recording is allowable, and the switch corresponding to the spot number has been operated. This output applied to one input of gate 354 causes this gate to have logic '0' as its output irrespective of the state of the input. Since this output is fed via diode 355 and terminal 356 to control the output of the equipment and via diode 357 and terminal 358 to control the chime generator (Figure 12) as described later no output can be obtained from the equipment during this state.

The output from gate 352 is fed also to the NOR gate 359 via inverter 360. With the equipment as described, i.e. tape stationary and spot to be bypassed, both inputs to gate 359 will be at logic '0' hence the output will be at logic '1'. This output is fed via terminal 361 to the timer 128 (Figure 11) which initiates tape drive after a short interval determined by resistor 362, causing the tape to run on to the next spot without playing back its output. The logic '0' from inverter 360 is fed via diode 363 and terminal 364 to he input of gate 168 (Figure 9) to allow paging announcements to be made even though the motor is running. Resistor 365 (which replaces a link shown in dotted line in Figure 9) limits the current to be sunk by inverter 360.

If the spot code is not one selected to be by-passed, is 10 or greater, or is coded so that local recording is inhibited, then the output of gate 352 will be logic '0' and the output of gate 354 will depend upon the state of its other input. As this input is derived from inverter 366 the output of gate 354 will be identical to the input to inverter 366. This input is the control voltage from the timer level converter 261 (Figure 11), which is now fed via terminal 367, inverter 366, gate 354 and diode 355 (which replaces the upper diode 282 Figure 11), to the interface relay driver 262 and analogue switch 192 (Figure 10). Thus in this condition the equipment operates normally, the spot starting at the end of the timer interval and the output being fed to the output socket. The control voltage is fed also to transistor 284 (Figure 12) via inverter 366, gate 354 and diode 357 (which replaces diode 287 (Figure 11)), in order to initiate the chime generator at the start of each spot played back.

Referring to Figure 16, an incomplete tape reset circuit is shown. This circuit allows the user to record part of a tape and, upon playback, cause the unit to run on after playing the last recorded message (spot) until the first message is available for replay.

The data from the data memory is copied into the data stores, 345 and 346, as described in the spot omission circuit (Figure 15). The outputs from the stores 345, 346 corresponding to the spot number code are fed to last spot detectors 368, 369 where the code is compared with the B.C.D. code for the 'last recorded message' which the user sets by means of last spot switches 370.

If the code read from the tape is less than or equal to the code set on the last spot switch the output from the last spot detector is a logic '0' which is applied to inverter 366 (Figure 15). The logic '0' iat this inverter input will cause the equipment to function normally, as described in the spot omission circuit.

If the code read from the tape is greater than the code set by the last spot switch the output of the last spot detector will be logic '1'. This is applied to the input of gate 352 via the inverter 366 and causes the tape to advance for all spots where local recording is not inhibited as described in the spot omission circuit. As with the spot omission circuit centrally pre-recorded messages cannot be missed, by setting the last spot switch to a code less than that of these messages.

WHAT WE CLAIM IS:—

1. A tape recording and playback system comprising means for recording information signals on a tape, means for recording digital signals on the tape to identify selected tape segments and any information signals recorded thereon, means for playing back the recorded digital signals, and means for providing system control signals dependent upon the played back digital signals, wherein the digital signal recording means comprises an astable timing oscillator, a parallel to serial register receiving clock pulses from the timing oscillator, switches for supplying a binary digital code to the paral-

lel inputs of the register, which digital code appears at the serial output of the register in response to received clock pulses, a data oscillator controlled by the serial output of the register to oscillate at a first or a second frequency in dependence upon the state of the serial output of the register, and a clock oscillator arranged to oscillate at a third frequency, the outputs of the data and clock oscillators being combined to provide a common output comprising a series of pulses at the first or second frequency separated by pulses at the third frequency.

2. A tape recording and playback system according to Claim 1, wherein the second frequency is zero.

3. A tape recording and playback system according to Claim 2, comprising a counter arranged to count clock pulses provided by the timing oscillator and to set the register to its parallel operation state after the binary digital code has been clocked through the register.

4. A tape recording and playback system according to Claim 3, comprising a timer triggered by the counter when the binary code has been clocked through the register, the timer when triggered maintaining the clock oscillator in its oscillating condition to provide an end of code signal.

5. A tape recording and playback system according to Claim 4, comprising a bistable circuit controlling the timing oscillator, the bistable being controlled by an initiate switch to turn on the timing oscillator and being controlled by the timer to turn off the timing oscillator when the end of code signal is generated.

6. A tape recording and playback system according to any preceding claim, wherein the control signal providing means comprises frequency selective switches each responsive to a respective one of the recorded pulse frequencies.

7. A tape recording and playback system according to Claim 6, comprising means for rendering the frequency selective switches unresponsive to signal absences of less than a predetermined period.

8. A tape recording and playback system according to Claim 7, wherein the digital signals are recored in the form of data pulses of one frequency and clock pulses of another frequency and two frequency selective switches are provided, the switch responsive to data pulses controlling a data pulse delay bistable feeding data pulses to a data memory register and the switch responsive to clock pulses applying clock pulses to the date memory register.

9. A tape recording and playback system according to Claim 6, 7, or 8, comprising a tape drive control circuit arranged to stop the tape when a digital signal is received.

10. A tape recording and playback system according to Claim 9, wherein the digital signals are terminated by a pulse the length of which is greater than the lengths of preceding pulses in the digital signals, and a long pulse detector is provided to activate the tape drive control circuit when the terminating pulse is received.

11. A tape recording and playback system according to any preceding claim, comprising an array of selector switches which when actuated provide respective outputs at one logic level, each said output being applied to a respective inverter and a respective NOR gate, and each NOR gate being connected to each of the inverters except that associated with the respective switch, whereby if only one switch is actuated a control output will appear at the output of the associated NOR gate, but if more than one switch is actuated no control outputs will appear at the outputs of any of the NOR gates.

12. A tape recording and playback system according to any preceding claim, comprising a timer adapted to activate a tape drive control circuit at preselected time intervals.

13. A tape recording and playback system according to any preceding claim, comprising a chime generator providing a sequence of notes when a tape drive circuit is deenergised.

14. A tape recording and playback system according to Claim 8, or any claim dependent upon Claim 8, wherein the outputs of the data memory register are fed to respective data stores, means are provided for detecting when a tape drive circuit is deenergised and for transferring data in the data memory register to the data stores when deenergisation of the tape drive circuit is detected, and means are provided for displaying the contents of the data stores.

15. A tape recording and playback system according to any preceding claim, comprising means for selecting a digital code, means for detecting a recorded digital code as a tape carrying the recorded code is driven, means for sensing when the selected and recorded digital codes correspond, and means for playing back information associated with the recorded digital code which corresponds with the selected digital code.

16. A tape recording and playback system according to claim 15, wherein the selecting means enables a sequence of digital codes to be selected and means are provided for playing back information associated with the selected sequence of digital codes.

17. A tape recording and playback system according to any preceding claim, wherein the information signals and digital signals are recorded on separate tape tracks.

18. A tape recording and playback system according to any one of claims 1 to 16, wherein the information signals and digital signals are recorded on the same tape track in different frequency bands.

19. A method controlling a tape recording

and playback system in dependence upon a tape which is being played back by a tape recording and playback machine which is a component of the system, wherein digital signals are recorded on the tape to identify selected tape segments and any information signals recorded thereon, the recorded digital signals are played back, and system-control-signals are provided in dependence upon the played back digital signals, wherein in order to generate said digital signals an astable timing oscillator provides clock pulses to a parallel to serial register, the parallel inputs of which are supplied with a binary digital code by switches, which digital code appears at the serial output of the register in response to the clock pulses, a data oscillator is controlled by the serial output of the register to oscillate at a first or a second frequency in dependence upon the state of the serial output of the register, a clock oscillator is arranged to oscillate at a third frequency and the outputs of the data and clock oscillators are combined to provide a common output comprising a series of pulses at the first or second frequency separated by pulses at the third frequency.

20. A tape recording and playback system substantially as hereinbefore described with reference to the accompanying drawings.

21. A method of controlling a tape recording and playback system substantially as hereinbefore described with reference to the accompanying drawings.

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AGENTS FOR THE APPLICANTS

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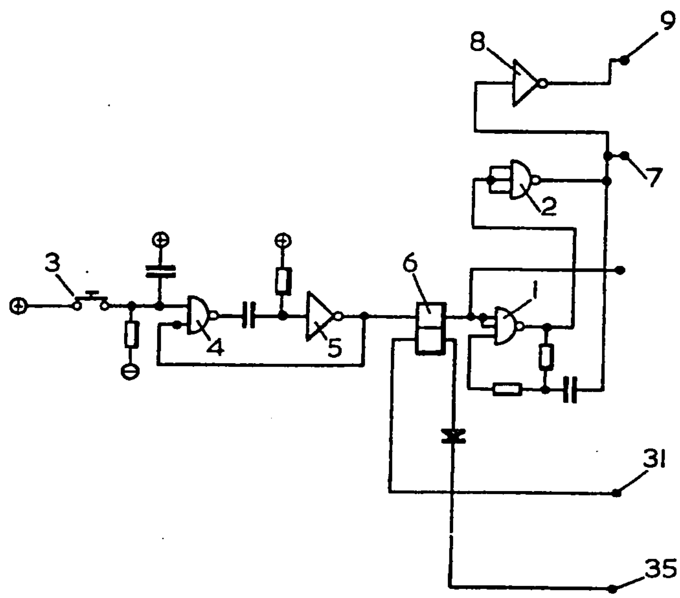

FIG. 1

1603828 COMPLETE SPECIFICATION

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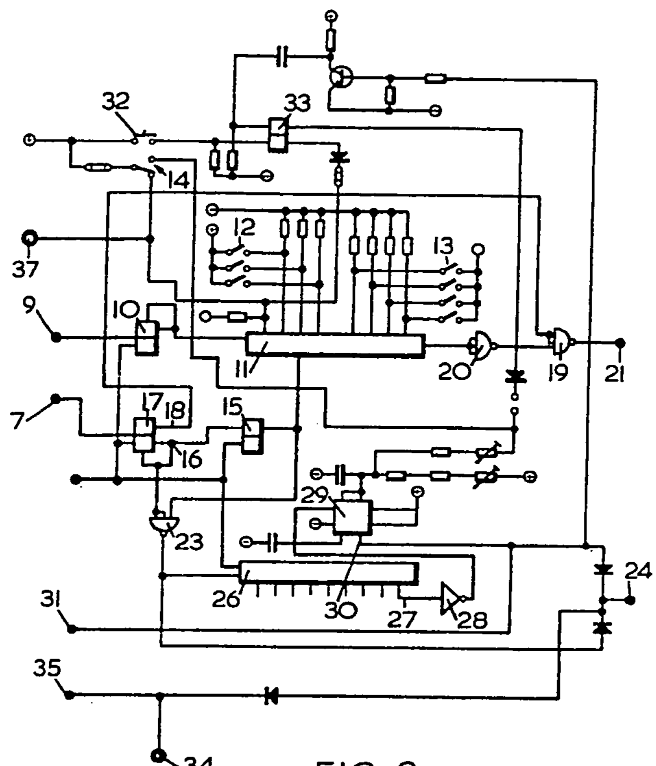

FIG. 2

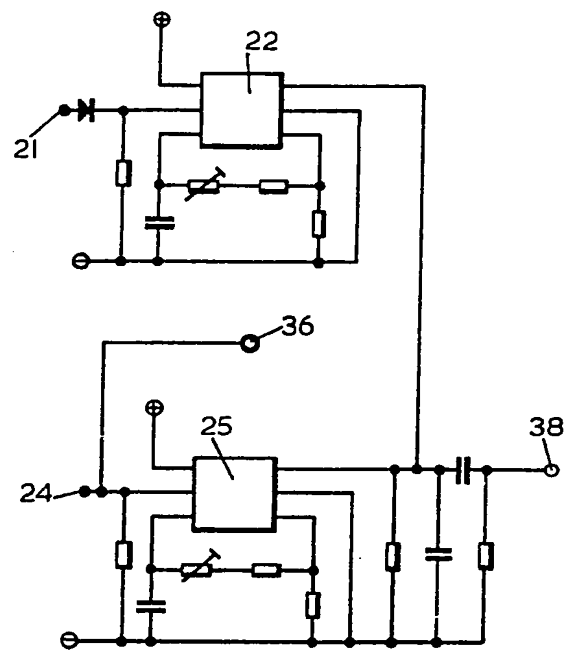

FIG. 3

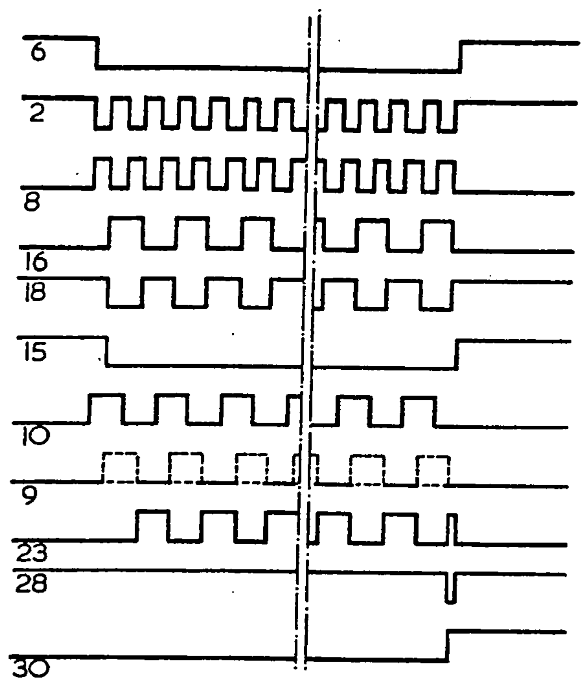

FIG.4

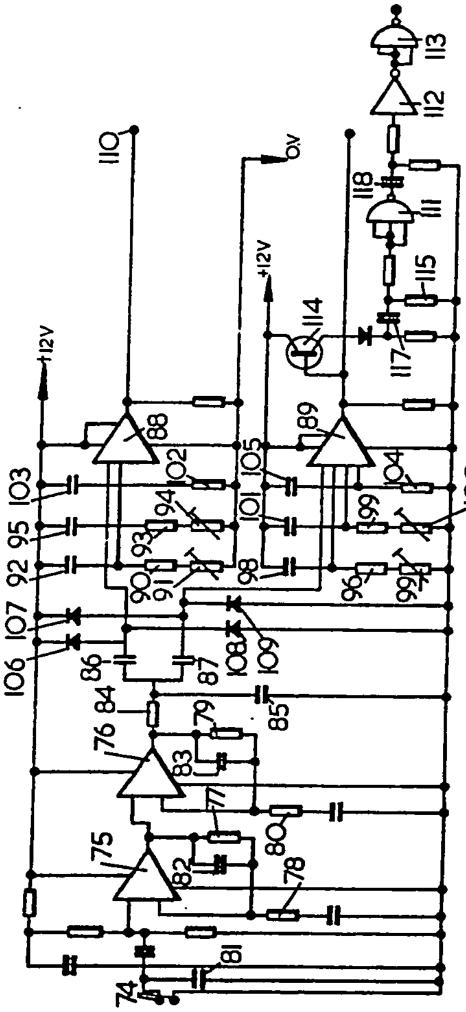
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FIG. 5

1603828 COMPLETE SPECIFICATION

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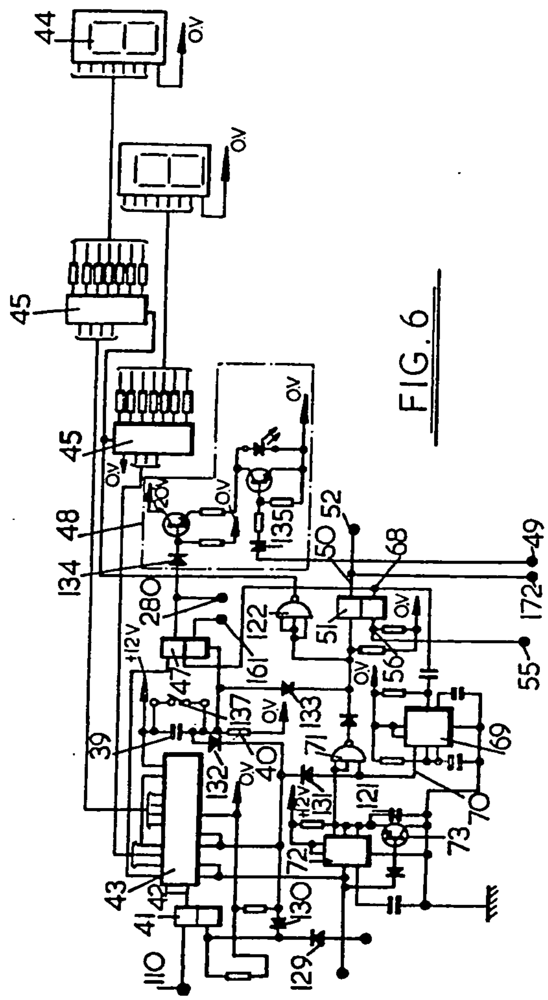

FIG. 6

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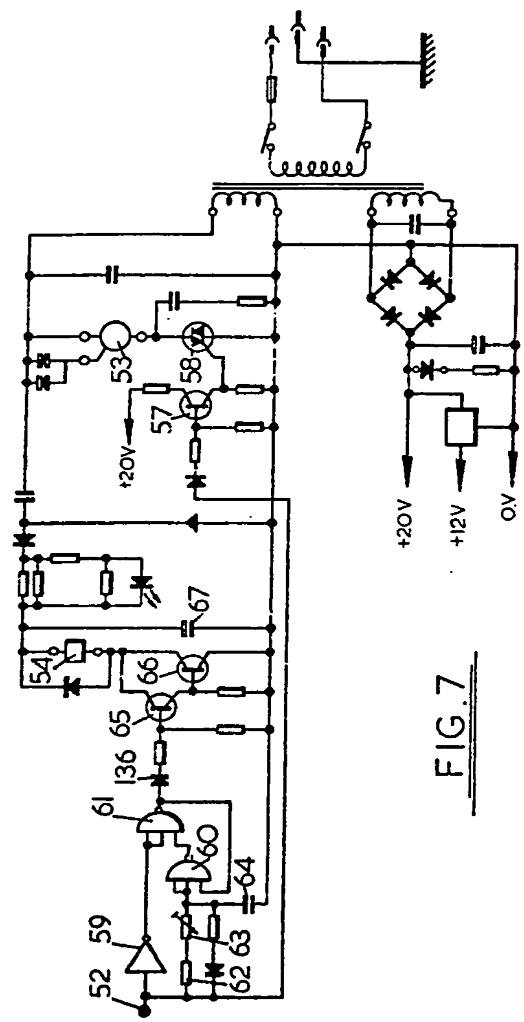

FIG.7

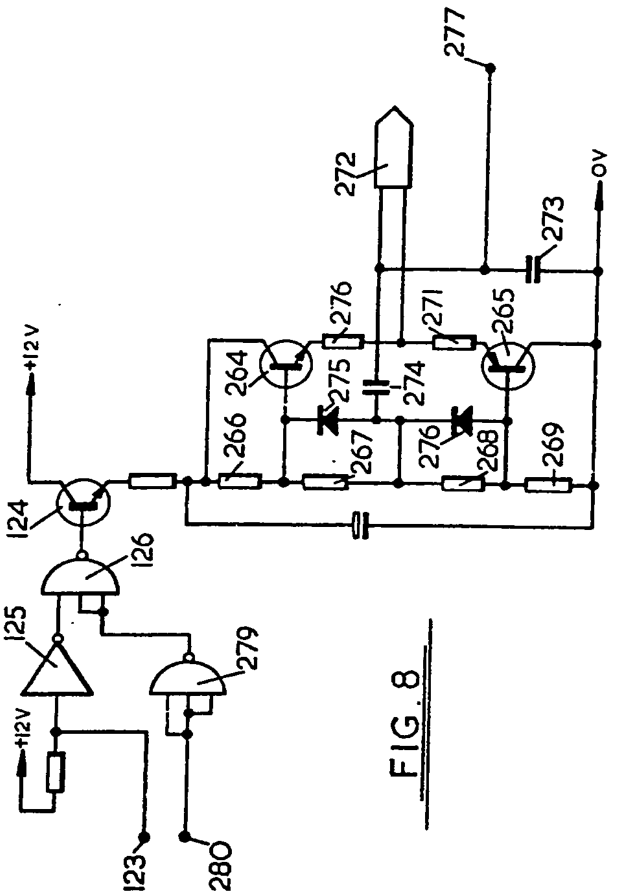
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FIG. 8

1603828 COMPLETE SPECIFICATION

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Sheet 9

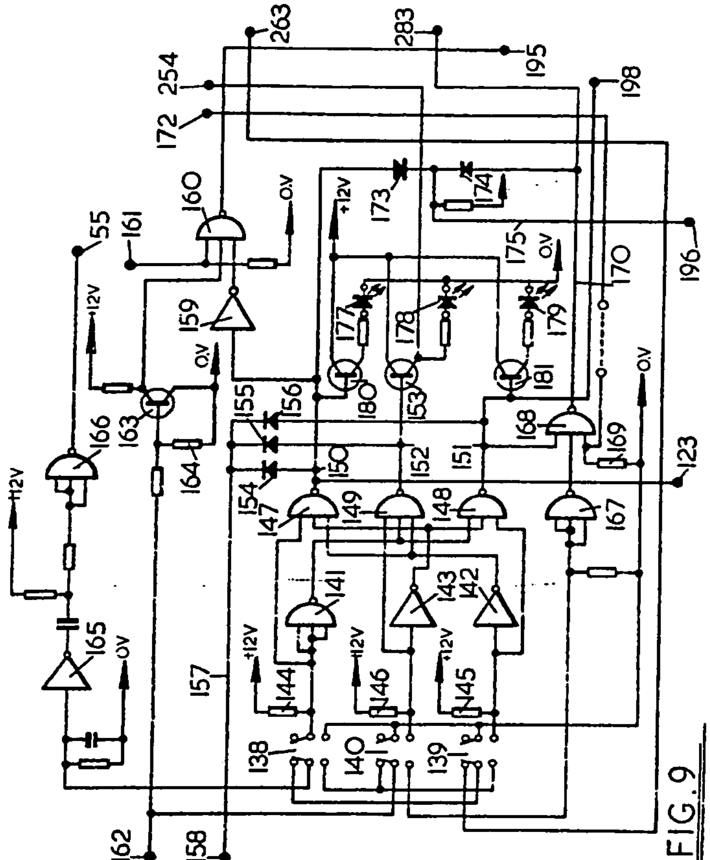

FIG. 9

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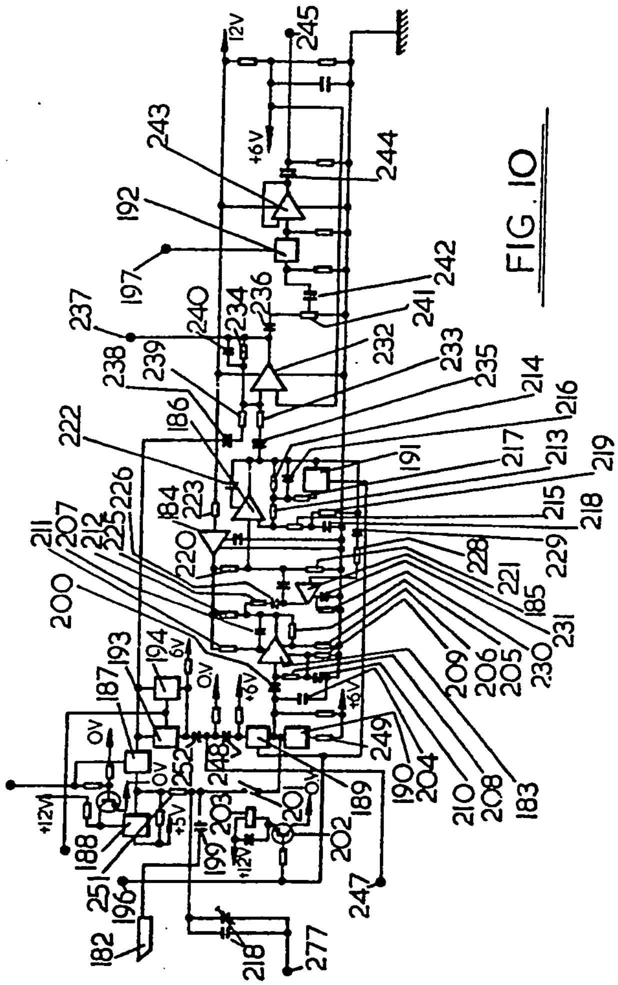

FIG. 10

1603828 COMPLETE SPECIFICATION

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Sheet 11

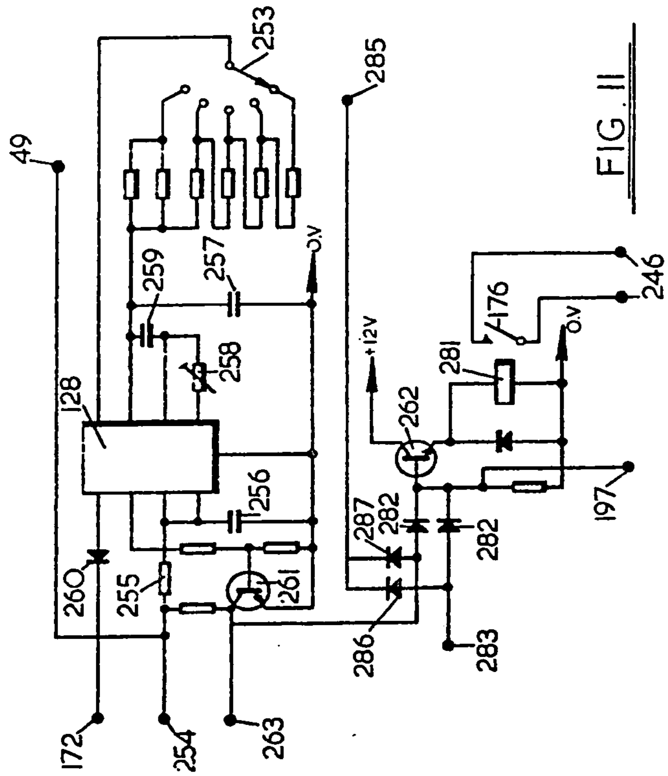

FIG. II

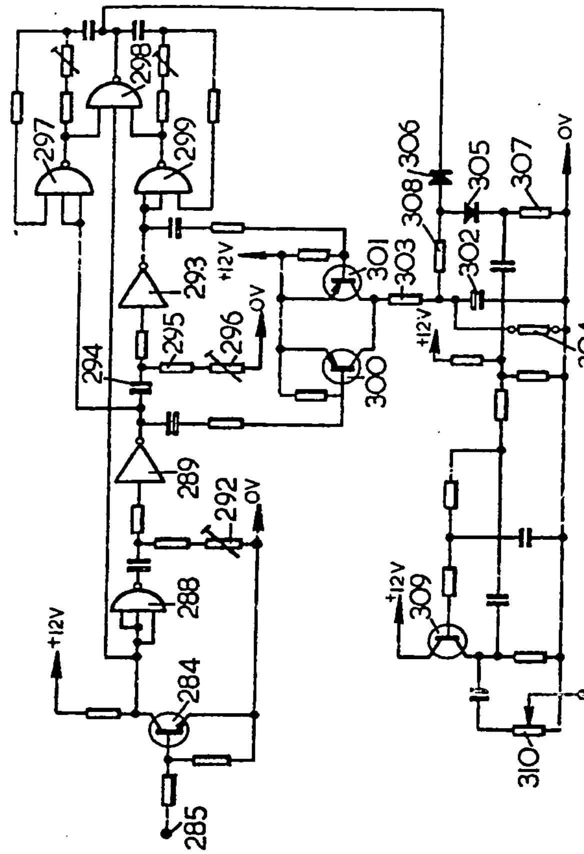
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FIG. 12

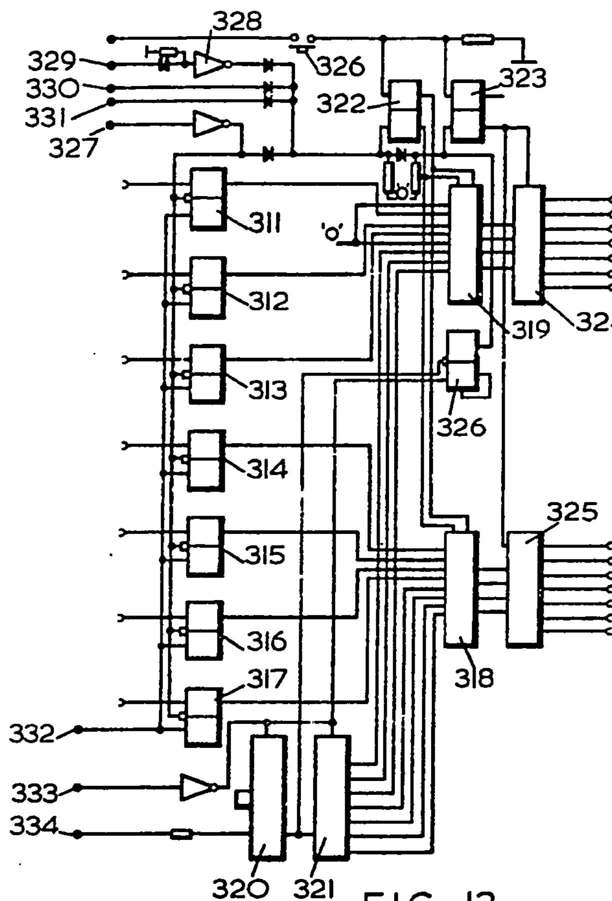
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FIG. 13

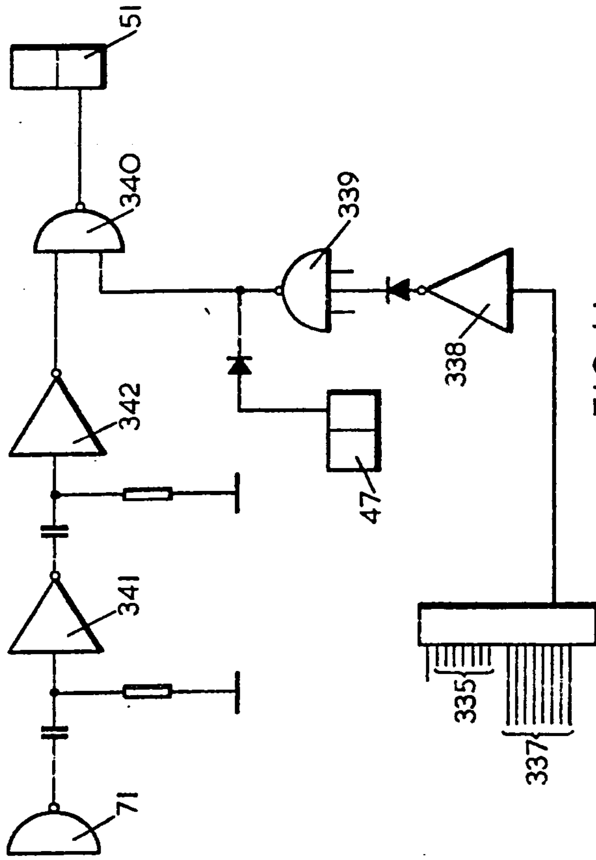
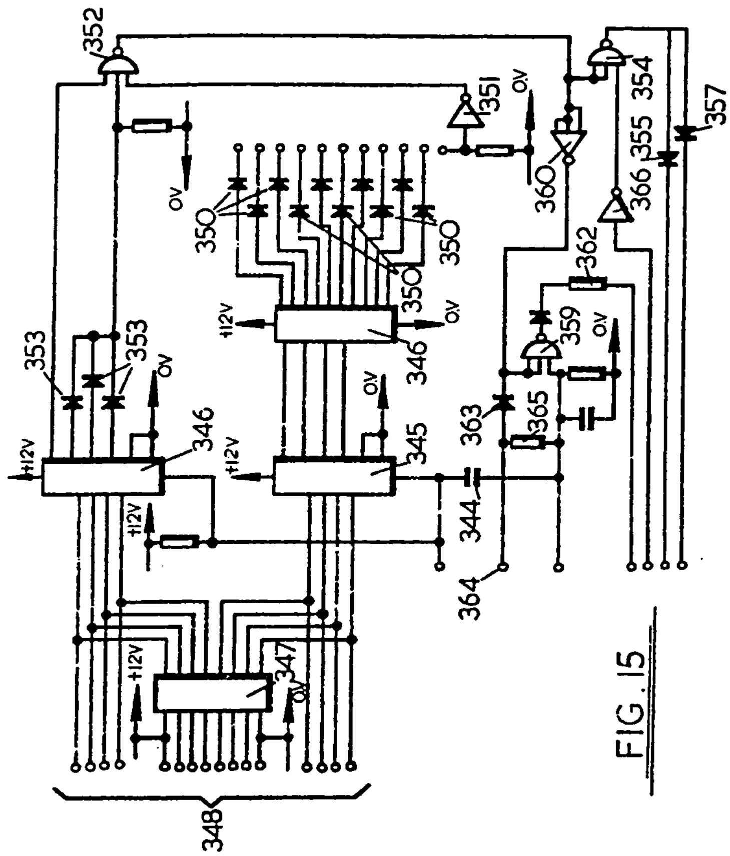


FIG. 14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348
+12V

FIG. 15

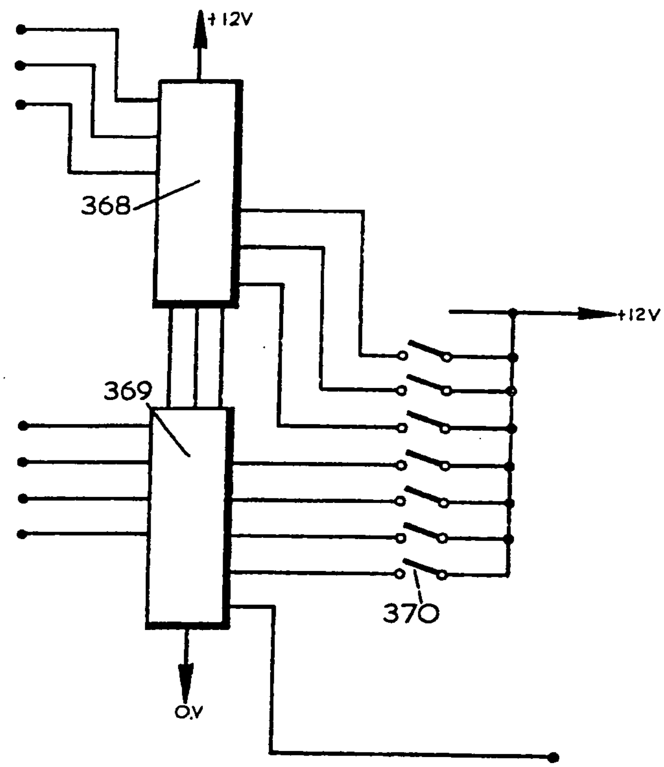

FIG.16